REMARKS

The Official Action mailed April 3, 2007, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Filed concurrently herewith is a *Request for Continued Examination*. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on October 23, 2003; and December 16, 2004.

Claims 1-8 and 12-27 are pending in the present application, of which claims 1-8 are independent. Claims 3 and 5-8 have been amended to better recite the features of the present invention. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

The Official Action rejects claims 1-8 and 12-19 as obvious based on the combination of U.S. Patent No. 2005/0087772 to Yamazaki. It further appears that the Official Action relies on Jaeger, "Introduction to Microelectric Fabrication," Volume 5, 1993, pages 18-19 and 91-95, to support the rejection. Although Jaeger is cited on Form PTO-892, it is unclear whether the Jaeger reference is intended to be part of the alleged *prima facie* case of obviousness. In any event, regarding independent claims 1, 2 and 4, the Applicant respectfully traverses the rejection because the Official Action has not made a *prima facie* case of obviousness. Regarding independent claims 3 and 5-8, the Applicant respectfully submits that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present application, as amended.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Regarding independent claims 1, 2 and 4, the prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Claims 1, 2 and 4 are directed to a method for manufacturing a semiconductor apparatus comprising the steps of forming a mask comprising a resist over a semiconductor to overlap with a portion of the semiconductor; adding an impurity element to the semiconductor in accordance with the mask; where an area of the mask is at most 15% of an area of the substrate. Claims 2 and 4 further recite an acceleration voltage of at leas 80kV. Claim 4 further recites that an area of the mask is at most 35% of an area of the substrate. For the reasons provided below, Yamazaki '772 and Jaeger, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

The Offical Action asserts the following (page 2, Paper No. 20070321):

> ... Yamazaki disclose forming a semiconductor over the substrate then forming a mask and then doping the substrate[.] Furthermore Yamazaki disclose the modulation of the implantation and the mask (see 0098). ... However, Yamazaki fails to disclose the mask precise parameters of the mask area and the implantation energy. It would have been obvious ... to make the mask 15% of the substrate area and use an acceleration voltage of at least 60keV, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. ... Furthermore the

use of a smaller mask are would enable one to dope more of the semiconductor also modulating the mask area is very well known in the art ....

The Applicant respectfully disagrees and traverses the assertions in the Official Action.

In a transistor, a source region or a drain region can be formed by adding an impurity using a mask. However, there are problems when a resist, which is generally used as a mask, is degassed by ion beam irradiation. Due to this, pressure in a treatment chamber is increased, it becomes impossible to irradiate the ion beam, and an injection amount of impurities has a margin of error. The present invention recognizes and solves the degassing problem by adjusting an area of a resist mask.

The Applicant respectfully submits that Yamazaki '772 and Jaeger, either alone or in combination, do not teach or suggest why one of ordinary skill in the art at the time of the present invention would have been concerned with adjusting an area of a resist mask when forming a mask comprising a resist over a semiconductor to overlap with a portion of the semiconductor, and when adding an impurity element to the semiconductor in accordance with the mask by a doping method.

Regarding independent claims 3 and 5-8, the prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended.

Independent claim 3 has been amended to recite forming a first semiconductor layer and a second semiconductor layer over a substrate; forming a first mask comprising a resist over the second semiconductor layer; adding a first impurity element having one conductivity to the first semiconductor layer in accordance with the first mask by a doping method; removing the first mask; forming a second mask comprising a resist over the first semiconductor layer; and adding a second impurity element having a conductivity different from the one conductivity to the second semiconductor layer in accordance with the second mask, where an area of at least one of the first mask and the second mask is at most 35% of an area of the substrate.

Independent claim 5 has been amended to recite forming a first semiconductor layer and a second semiconductor layer over a substrate; forming a first gate electrode over the first semiconductor layer with a first gate insulator therebetween; forming a second gate electrode over the second semiconductor layer with a second gate insulator therebetween; forming a first mask comprising a resist over the second semiconductor layer; adding an n-type impurity element to the first semiconductor layer in accordance with the first mask and the first gate electrode by a doping method with acceleration voltage of at least 60kV; removing the first mask; forming a second mask comprising a resist over the first semiconductor layer; and adding a p-type impurity element to the second semiconductor layer in accordance with the second mask and the second gate electrode by a doping method with acceleration voltage of at least 80kV, where an area of the first mask is at most 20% of an area of the substrate, and an area of the second mask is at most 15% of an area of the substrate.

Claim 6 is similar to claim 5 and further recites heating the masks, and 40% and 35% instead of 20% and 15%, respectively.

Claim 7 is similar to claim 5 and further recites a current density of at least $15\mu A/cm^2$.

Claim 8 includes the features of claims 6 and 7.

The Applicant respectfully submits that Yamazaki '772 and Jaeger, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

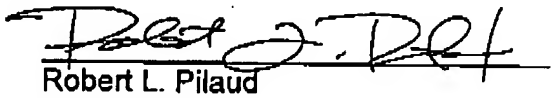
Since Yamazaki '772 and Jaeger do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

The Official Action rejects dependent claims 20-27 as obvious based on the combination of Yamazaki '772, Jaeger and U.S. Patent Application Publication No. 2005/0011455 to Yamamoto.

Yamamoto does not cure the deficiencies in Yamazaki and Jaeger. The Official Action relies on Yamamoto to allegedly teach the features of the dependent claims. Specifically, the Official Action relies on Yamamoto to allegedly teach a substrate with an area of one square meter (page 3, Paper No. 20060320). However, regarding claims 1, 2 and 4, Yamazaki, Jaeger and Yamamoto, either alone or in combination, do not teach or suggest why one of ordinary skill in the art at the time of the present invention would have been concerned with adjusting an area of a resist mask when forming a mask comprising a resist over a semiconductor to overlap with a portion of the semiconductor, and when adding an impurity element to the semiconductor in accordance with the mask by a doping method. Also, Yamazaki, Jaeger and Yamamoto, either alone or in combination, do not teach or suggest the above-referenced features of the amended independent claims 3 and 5-8. Since Yamazaki and Jaeger and Yamamoto do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



Robert L. Pilaud
Reg. No. 53,470

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789